UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/575,822	04/12/2006	Richard Allan Tuck	920670-103085	5265

23644 7590 05/22/2008
BARNES & THORNBURG LLP
P.O. BOX 2786
CHICAGO, IL 60690-2786

EXAMINER	
BOWMAN, MARY ELLEN	

ART UNIT	PAPER NUMBER
4174	

NOTIFICATION DATE	DELIVERY MODE
05/22/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patent-ch@btlaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/575,822	TUCK, RICHARD ALLAN	
	Examiner	Art Unit	
	MARY ELLEN BOWMAN	4174	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) *13,22 and 24-43* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12, 14-21, 23, and 44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

2. Claim 11 is objected to because of the following informalities: Reference to "the channels of the hop-plate" lacks proper antecedent basis. For purposes of examination, the channels are considered to be the emitting areas. Claim 18 is objected to because it claims "on said hop-plate and/or flue-plate," and either "and" or "or" should be chosen. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5, 11-15, 18, 19, and 44 are rejected under 35 U.S.C. 102(b) as being anticipated by Deguchi et al., USPN 6,400,091 B1, published 04 June 2002 (hereinafter referred to as "Deguchi").

5. Regarding claim 1, Deguchi teaches a Hop-FED structure (e.g., col 1, line 17; "field emission (FE)-type [cold cathode electron source]") comprising: a substrate (e.g., col 8, line 44; "a first substrate 41"); emitter areas on said substrate (e.g., col 8, line 51; "an electron emission member 14"); a hop-plate disposed over said substrate and emitter areas (e.g., col 8, line 53; "an

insulating layer 47"; see also Figure 3 below, insulating layer 47 is disposed on substrate and emitter areas; NOTE: Hop-plate is not a well known term of art within the relevant field, therefore this element has been defined within the parameters set forth in the specification.) with a surface of the hop-plate opposing said substrate and emitter areas (e.g., Figure 3 below, the top surface of the insulating layer 47 is opposing the substrate 42 and emitter areas 14); and an electrically conductive layer formed on said surface of the hop-plate (e.g., col 8, lines 53-54; "a control electrode 48 formed on the insulating layer 47").

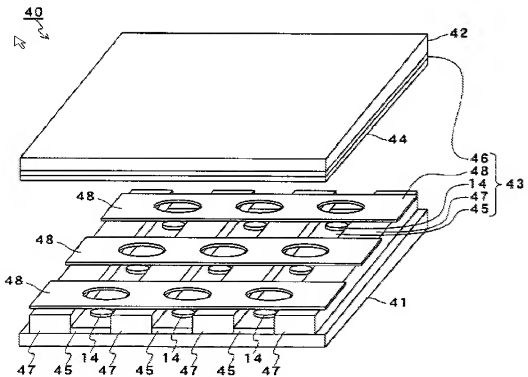


Fig.3

6. Regarding claim 2, Deguchi teaches the invention as explained above regarding claim 1, and further teaches said surface [of the hop-plate] is formed with projections that space the remainder of the hop-plate from said substrate and emitter areas (e.g., Figure 3 above, insulating

layer 47 [hop-plate] is formed as pillars or ribs so that the remainder of the layer is separated from the substrate and emitter areas and only the bottom surface is in contact with the substrate).

7. Regarding claim 3, Deguchi teaches the invention as explained above regarding claim 2, and further teaches said projections are formed as pillars or ribs (e.g., Figure 3 above, insulating layer 47 [hop-plate] is formed as pillars or ribs so that the remainder of the layer is separated from the substrate and emitter areas and only the bottom surface is in contact with the substrate).

8. Regarding claim 4, Deguchi teaches the invention as explained above regarding claim 2, and further teaches said electrically conductive layer (e.g., "control electrode 48") is provided on said projections (e.g., col 8, lines 53-54; "a control electrode 48 formed on insulating layer 47 [hop-plate projections]").

9. Regarding claim 5, Deguchi teaches the invention as explained above regarding claim 2, and further teaches said electrically conductive layer (e.g., "control electrode 48") is not provided on said projections (e.g., Figure 3 above, part of each control electrode 48 crosses between the insulating layers 47 and at those points is not on the projections).

10. Regarding claim 11, Deguchi teaches the invention as explained above regarding claim 1, and further teaches said electrically conductive layer (e.g., "control electrode 48") extends partially within the channels (i.e., the space between the insulating layers 47) of the hop-plate (e.g., Figure 3 above, part of each control electrode 48 crosses between the insulating layers 47 and at those points is extending within the channels of the hop-plate [insulating layer 47]).

11. Regarding claim 12, Deguchi teaches the invention as explained above regarding claim 1, and further teaches said electrically conductive layer (e.g., "control electrode 48") is connected to means for holding said layer at a predetermined potential (e.g., col 9, lines 52-56; "a scan

driver 51 is electrically connected to the control electrodes 48...[and] the scan driver 51 applies a scanning signal for successively driving m rows of control electrodes 48").

12. Regarding claim 14, Deguchi teaches a Hop-FED structure (e.g., col 1, line 17; "field emission (FE)-type [cold cathode electron source]") comprising: a cathode with emitter areas (e.g., col 8, lines 49-52; "each electron emission element 43 includes a cathode 45 disposed on the first substrate 41, [and] an electron emission member 14 disposed on the cathode 45"); an anode arranged to receive electrons emitted from the cathode (e.g., col 8, lines 52-53; "an anode 46 formed on the second substrate 42 [opposite the first substrate 41]"); a hop-plate disposed between the cathode and anode (e.g., col 8, line 54; "insulating layer 47"; see also Figure 3 below, insulating layer 47 [hop-plate] is disposed between the cathode 45 and anode 46); spacer means arranged to provide a space between said cathode and anode (e.g., "insulating layer 47", NOTE: The insulating layer 47 serves as both a hop-plate and a spacer means for separating the cathode and anode.); and gettering material disposed in said space (e.g., col 9, lines 17-19; "a getter film…is formed at a predetermined position in the airtight container [between the first and second substrates]").

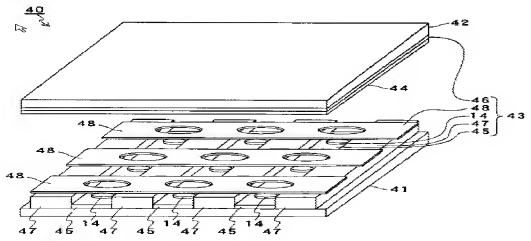


Fig. 3

13. Regarding claim 15, Deguchi teaches the invention as explained above regarding claim 14, and further teaches said spacer means (e.g., "insulating layer 47") comprises projections provided on one or both faces of said hop-plate (e.g., Figure 3 above, insulating layer is formed as rib-like projections on either or both of the top and bottom face of the hop-plate [insulating layer 47]).

14. Regarding claim 18, Deguchi teaches the invention as explained above regarding claim 15, and further teaches said spacer means (e.g., "insulating layer 47") are formed as pillars or ribs on said hop-plate and/or flue-plate (e.g., Figure 3 above, insulating layer is formed as rib-like projections on either or both of the top and bottom face of the hop-plate [insulating layer 47]; NOTE: The broadest reasonable interpretation of "and/or flue-plate" is determined to be "or flue-plate").

15. Regarding claim 19, Deguchi teaches the invention as explained above regarding claim 14, and further teaches said gettering material forms a distributed getter (e.g., col 9, line 17; "a getter film").

16. Regarding claim 44, Deguchi teaches a Hop-FED structure (e.g., col 1, line 17; "field emission (FE)-type [cold cathode electron source]") comprising: a cathode having a substrate and emitter areas on said substrate (e.g., col 8, lines 49-52; "each electron emission element 43 includes a cathode 45 disposed on the first substrate 41, [and] an electron emission member 14 disposed on the cathode 45"); an anode arranged to receive electrons emitted from the cathode (e.g., col 8, lines 52-53; "an anode 46 formed on the second substrate 42 [opposite the first substrate 41]"); a hop-plate disposed over said substrate and emitter areas, between the cathode and anode, with a surface of the hop-plate opposing said substrate and emitter areas (e.g., col 8,

line 53; "an insulating layer 47"; see also Figure 3 below, insulating layer 47 is disposed on substrate and emitter areas, insulating layer 47 [hop-plate] is disposed between the cathode 45 and anode 46, and the top surface of insulating layer 47 [hop-plate] opposes the substrate and emitter areas); an electrically conductive layer formed on said surface of the hop-plate (e.g., col 8, lines 53-54; "a control electrode 48 formed on the insulating layer 47"), spacer means arranged to provide a space between said cathode and anode (e.g., "insulating layer 47", NOTE: The insulating layer 47 serves as both a hop-plate and a spacer means for separating the cathode and anode.); and gettering material disposed in said space (e.g., col 9, lines 17-19; "a getter film…is formed at a predetermined position in the airtight container [between the first and second substrates]").

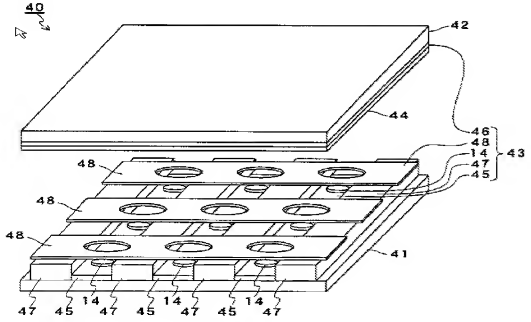


Fig.3

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deguchi in view of Jones et al., USPN 6,255,771 B1, published 03 July 2001 (hereinafter referred to as "Jones").

19. Deguchi teaches the invention as explained above regarding claim 1, but fails to teach the composition or resistivity of the electrically conductive layer.

20. Regarding claim 6, Jones teaches said electrically conductive layer (e.g., col 10, lines 3-5; "a resistive coating 1100 [conductive layer] may be provided on the upper surface of the surface insulator layer 1000 [hop-plate]") is of a material of high electrical resistivity (e.g., col 11, lines 2-4; "in terms of sheet resistivity, the value must be greater than 10^9 Ohms/square").

21. Regarding claim 7, Jones teaches said material has a surface resistivity in the range 10^7 to 10^{11} ohms/square (e.g., col 11, lines 2-4; "in terms of sheet resistivity, the value must be greater than 10^9 Ohms/square").

22. Regarding claim 8, Jones teaches said material has a surface resistivity in the range 10^8 to 10^{10} ohms per square (e.g., col 11, lines 2-4; "in terms of sheet resistivity, the value must be greater than 10^9 Ohms/square").

23. Regarding claim 9, Jones teaches said material has a surface resistivity of substantially 10^9 ohms per square (e.g., col 11, lines 2-4; "in terms of sheet resistivity, the value must be greater than 10^9 Ohms/square").

24. Regarding claim 10, Jones teaches said material is selected from the group comprising amorphous silicon and silver doped silica (e.g., col 10, lines 14-16; "the resistive coating 1100 [conductive layer] may comprise…undoped silicon").

25. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a material with high resistivity as the conductive layer overlying the hop-plate, because the high resistivity allows for efficient and effective electron beam focusing, which results in a better image quality (Jones: col 10, lines 32-38; "the surface potential…will provide focusing"). Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to optimize the range and value of the resistivity, because that involves only routine skill in the art. *In re Aller*, 105 USPQ 233; *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Thus, reconstruction is desirable as taught by the prior art.

26. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deguchi in view of Jeong et al., USP App. Pub. No. 2003/0178934 A1, published 25 September 2003 (hereinafter referred to as "Jeong").

27. Deguchi teaches the invention as explained above regarding claim 14, but fails to teach a flue-plate.

28. Regarding claim 16, Jeong teaches a flue-plate (e.g., [0083]; "convergence electrodes 25") between said hop-plate (e.g., [0083]; "insulating layer 22") and anode (e.g., [0067]; "an

anode plate 1"; see Figures 5 and 6 below, convergence electrodes 25 [flue-plates] are between the insulating layer 22 [hop-plate] and anode 1).

FIG. 5

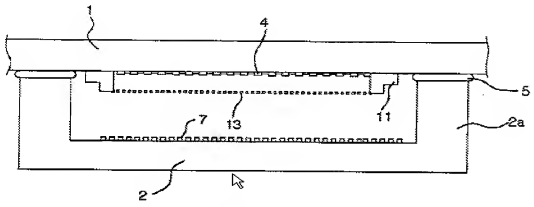
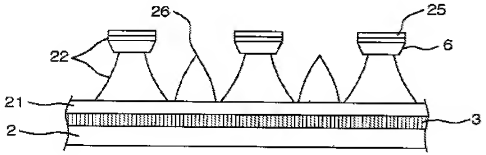


FIG. 6



29. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a flue-plate in the image display construction in order to improve focusing of the electron beam, thereby improving image quality (Jeong: [0084]; "convergence electrodes for compensating the spread phenomenon of the electron beams"). Thus, reconstruction is desirable as taught by the prior art reference.

30. Regarding claim 17, Deguchi and Jeong teach the invention as explained above regarding claim 16, and Deguchi further teaches projections provided on one or both faces of said flue-

plate (e.g., "insulating layer 47" is formed as rib-like projections on either or both of the top and bottom face of the hop-plate [insulating layer 47], which would then have a flue-plate overlying conductive layer 48, as taught by Jeong; see Figure 3 below).

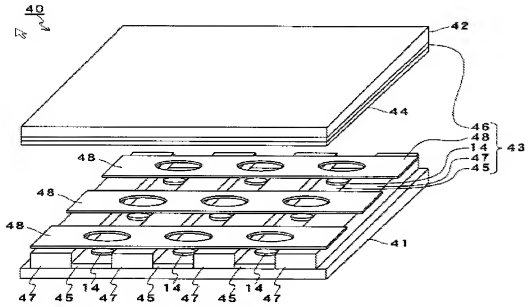


Fig. 3

31. Claims 20, 21, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deguchi in view of Abe et al., USPN 6,624,586 B2, published 23 September 2003 (hereinafter referred to as "Abe").

32. Regarding claims 20 and 21, Deguchi teaches the invention as explained above regarding claim 14, but fails to teach specific details regarding the gettering.

33. Regarding claim 20, Abe teaches said gettering material comprises a non-evaporated getter (e.g., col 7, lines 7-9; "the getter 9 may be an evaporative getter or unevaporative getter, the unevaporative getter which can be formed in a wider area is preferably used").

34. Regarding claim 21, Abe teaches said gettering material (e.g., "getter 9") comprises an alloy containing at least one Group IV metal (e.g., col 5, lines 31-33; "the getter is preferably a metal or alloy containing at least any one of Ti, Zr, [and] Hf"; Note: Ti, Zr, and Hf are Group IV metals.).

35. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a getter material of the above described type in order to achieve the characteristic absorbances associated with said materials, which thereby improves the vacuum in the display device (Abe: col 5, 30-31; "the getter in each invention described above has characteristics of absorbing substances in the atmosphere"). Thus, reconstruction is desirable as taught by the prior art reference.

36. Regarding claim 23, Deguchi teaches the invention as explained above regarding claim 14, and further teaches the structure is sealed by a glass-frit seal that is spaced from said gettering material (e.g., col 9, lines 9-12; "the substantially vacuum state of the airtight container can be achieved by sealing a connecting portion of each component member, for example, with frit glass"). Deguchi fails to teach a conductive member electrically connected to gettering material.

37. Regarding claim 23, Abe teaches a conductive member that is compatible with said glass-frit and extends from outside the structure, though said glass-frit seal and to said gettering material, to which it is electrically connected (e.g., col 4, lines 22-31; "the getter is electrically connected to a wiring line such that the getter is in contact with the wiring line"; col 4, lines 39-41; "[the wiring line is] the electrical path extending from the driving circuit [outside the structure] to the electron-emitting device [the structure]").

38. It would have been obvious to one of ordinary skill in the art at the time the invention was made to electrically connect the getter material to an outside electrical source in order to decrease characteristic variations and improve image uniformity (Abe: col 4, lines 47-48; "almost no characteristic variations, and high uniformity"). Thus, reconstruction is desirable as taught by the prior art reference.

Conclusion

39. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARY ELLEN BOWMAN whose telephone number is (571)270-5383. The examiner can normally be reached on Monday-Thursday, 6:30 a.m.-5:00 p.m. EST.

40. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly D. Nguyen can be reached on (571) 272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

41. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. B./
Examiner, Art Unit 4174

/Kimberly D Nguyen/
Supervisory Patent Examiner, Art Unit 4174